

In the Claims:

Please amend claims 1-4, 6-8, 10-15 and 17 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) A testing device for testing a phase locked loop having a power supply input, said testing device comprising:

a power supply unit for providing a power supply signal having a variation profile to the power supply input of the phase locked loop, wherein a width and height of said variation profile are formed in such a way, that the voltage controlled oscillator is prevented from outputting an oscillating output signal, and wherein a means for disabling a feedback signal, from the voltage controlled oscillator to a phase comparator of the phase locked loop, is disabled such that said phase locked loop is ~~operated~~ in an open loop mode;[[,]] and

a meter for measuring a measurement signal of the phase locked loop, while said power supply signal is provided to the power supply input.

2. (Currently amended) The testing device for testing a phase locked loop device according to claim 1, said ~~phase locked loop (PLL) having phase comparator and said phase comparator (10)~~ having a feedback input and a reference input, wherein both said feedback input (U_{fb}) and said reference input (U_{ref}) are connected to ground.

3. (Currently amended) The testing device for testing a phase locked loop according to claim 1, further comprising a periodic signal generator for providing a periodic input signal, wherein the phase comparator has a feedback input and a reference input, and wherein the periodic signal generator provides the periodic input signal having the same frequency to said feedback input (U_{fb}) and to said reference input (U_{ref}).

4. (Currently amended) The testing device for testing a phase locked loop device according to claim 1, wherein said meter is adapted to measure at least one of a current (I_{DD}) provided to ~~at least one of the following:~~ the power supply input, an output voltage

of the phase locked loop an output voltage, and an oscillator control voltage of the phase locked loop.

5. (Previously presented) The testing device for testing a phase locked loop device according to claim 1, wherein said power supply unit is adapted to provide a periodic power supply signal.

6. (Currently amended) The testing device for testing a phase locked loop device according to claim 3 [[1]], wherein the power supply unit is adapted to provide a periodic power supply signal, and wherein the periodic power supply signal provided by the power supply unit and the periodic input signal provided by the periodic signal generator ~~are both adapted to provide periodic signals having~~ have the same frequency.

7. (Currently amended) The testing device for testing a phase locked loop device ~~according to one of claims 1 to 6~~, according to claim 3 [[1]], wherein the power supply unit and the periodic signal generator are both adapted to provide periodic signals having a phase difference between the periodic power supply signal (~~VDD~~) and the periodic input signal is equal to 0, $T/4$ or $3T/4$, T being a period of both said periodic power supply signal (~~VDD~~) and said periodic input signal.

8. (Currently amended) The testing device according to claim 1 [[4]], wherein the meter is adapted to measure a current provided to the power supply input, and further comprising

a high pass filter for filtering the current (~~IDD~~) provided to the power supply input, and

an integrator for integrating the filtered power supply current (~~IDD~~), wherein the integrated power supply current is indicative of a defective phase locked loop.

9. (Previously presented) A phase locked loop comprising the testing device according to claim 1.

10. (Currently amended) Method for testing a phase locked loop (PLL) having a power supply input, comprising the steps:

operating the phase locked loop in an open loop mode

providing a power supply signal having a variation profile to the power supply input of the phase locked loop, wherein a width and height of said variation profile are formed in such a way, that the voltage controlled oscillator is prevented from outputting an oscillating output signal, and

measuring a measurement signal of the phase locked loop, while said power supply signal is provided to the power supply input of the phase locked loop.

11. (Currently amended) Method for testing a phase locked loop device (PLL-device) according to claim 10, wherein said variation profile of the power supply signal has a ascending edge, said ascending edge being short enough (T_{rise}) to prevent the voltage controlled oscillator (VCO) from outputting an oscillating output signal.

12. (Currently amended) Method for testing a phase locked loop device according to claim 10, wherein said variation profile of the power supply signal has a descending edge, said descending edge being short enough (T) to prevent the voltage controlled oscillator (VCO) from outputting an oscillating output signal (U_{out}).

13. (Currently amended) Method for testing a phase locked loop device according to claim 10, said phase locked loop (PLL) having a phase comparator and said phase comparator (Φ) having a feedback input (U_{fb}) and a reference input (U_{ref}), wherein both said feedback input (U_{fb}) and said reference input (U_{ref}) are connected to ground.

14. (Currently amended) Method for testing a phase locked loop device according to claim 10, wherein the phase locked loop includes a phase comparator that has a feedback input and a reference input, and wherein said feedback input and said reference input receive an identical periodic input signal.

15. (Currently amended) Method for testing a phase locked loop device according to claim 10, wherein the measurement signal is one of a current provided to the power supply input, an output voltage of the phase locked loop and/or an oscillator control voltage of the phase locked loop.

16. (Previously presented) Method for testing a phase locked loop device according to claim 10, wherein the power supply signal is a periodic voltage signal.

17. (Currently amended) Method for testing a phase locked loop device according to claim 14 [[15]], wherein the power supply signal is a periodic voltage signal, and wherein the periodic power supply signal and the periodic input signal to the reference input have the same frequency.

18. (Previously presented) Method for testing a phase locked loop device according to claim 17, wherein a phase difference between the periodic power supply signal and the periodic input signal is equal to 0, $T/4$ or $3T/4$, T being a period of both said periodic power supply signal and said periodic input signal.